Demonstrating Software Debug and Calibration Tools Utilizing the Nexus 5001 Standard

November 7, 2013
Welcome

Jane Celusak is a program manager supporting industry consortia on behalf of IEEE-ISTO including Nexus 5001 Forum. Jane works closely with the industry consortia leadership to develop new initiatives to support the strategic directions of organization and acts as a liaison between programs and other IEEE-SA support functions.

Jane has over 15 years’ experience in business and organizational development and external, customer and foundation relationship management. She has a MA in Public Policy and International Affairs.
Let’s Get Started!
Randy Dees

Randy Dees is a Senior Member of the Technical Staff at Freescale Semiconductor, working in the 32-bit Automotive Microcontroller Applications group supporting highly integrated advanced MCUs with embedded Flash memory.

He graduated from the University of Houston in December 1980 and began working at Motorola Semiconductor in January 1981. Motorola later spun the semiconductor group off as Freescale.

He has worked in both Product Engineering and Application supporting 8- to 32-bit microprocessors, integrated circuits for telecommunications, and 32-bit microcontrollers.

He has been working with Nexus-based MCUs since 1999 and has been either the co-chairman or the chairman of the IEEE-ISTO 5001 Nexus Consortium’s technical subcommittee since 2000.
Introduction

Nexus 5001 Forum
What is Nexus?

• Nexus is an industry standard debug standard for embedded microcontrollers.

• Growing out of a white paper written in 1998 from Freescale (then part of Motorola) along with Agilent Technologies (then HP) on a new debug standard, the Nexus Consortium joined forces with the IEEE-ISTO to release the first version of the standard, the IEEE-ISTO 5001-1999.

  • The standard was updated in 2003 to address enhancements and minor oversights (IEEE-ISTO 5001-2003).
  • An additional update was released in 2012 that adds support for the IEEE 1149.7 and Nexus messaging over an Aurora protocol link.

• The standard covers not only the debug protocol but also the pin interface and connectors, driving a new level of standardization

• To date, Nexus is implemented on MCU devices from several semiconductor companies on a wide variety of core types.

• Information on the Nexus Consortium can be obtained at www.nexus5001.org
The Nexus standard defines debug from Class 1 (static debug) all the way through to Class 4 with memory substitution and port replacement.
Nexus Members

- ATI
- ERICSSON
- ETAS
- Freescale
- Fulcware Corporation
- GM
- SYNOPSYS
- Green Hills Software, Inc.
- HDL Dynamics SoC Solutions
- Lauterbach Development Tools
- pls Development Tools
- Renesas
- Samtec
- McMaster University
- The University of Alabama in Huntsville
- Technische Universität Dresden
Agenda

- Introduction of Webinar contents and presenters - Jane Celusak, IEEE-ISTO
- Description of GM tool set; debugger, trace, M/C, RPC - Norm D’Amico – GM
- Lauterbach debugger + high speed trace demonstration - Udo Zoettler – Lauterbach
- M/C tool Demo, bypass + e-hooks demo and Multi tool use case – M/C + debugger/trace arbitration demo - Steve Rosenthal-ETAS
- Overview of IC’s supporting the Nexus 5001 Standard- Randy Dees, Freescale Semiconductor
- Q+A - Jane Celusak, IEEE-ISTO
Norm D'Amico is a Staff Engineer at General Motors working as a Team Leader in Global Powertrain ECU Development Tools.

- Norm works with the Tier-1 ECU suppliers and the Tier-2 tool suppliers to insure that GM's requirements are implemented properly on development ECUs. Norm has also worked in tool development and software integration roles while at GM.

- Prior to GM, Norm held several positions at ERIM (since acquired by General Dynamics) in the development of electronic hardware and software for synthetic aperture radar (SAR) systems.

- Norm received his B.S. in Electrical Engineering from Wayne State University in 1986, and has been involved in embedded electronic systems his entire career.
GM Tool Set

Norm D’Amico, General Motors
Opening Remarks

• Today’s material is a natural progression from the information that was presented at last year’s webinar (Use of Nexus Based Software Development Tools for Powertrain ECUs)

• The focus today will be to demonstrate some of the Nexus based development tools that are currently being used in industry
GM Tools Overview

- GM Powertrain has developed instrumentation strategies that are used across entire generations of ECU programs, including:
  - ECMs (Engine Control Modules)
  - TCMs (Transmission Control Modules)
  - Hybrids (Hybrid Control Modules)

- The Nexus-based instrumentation strategies have promoted reuse of the development tools and have helped GM to save both time and money.
GM Tools Overview

- There are 3 primary tool sets used in the development of ECU software and calibration at GM
  - Software debugging / trace tools
  - Measurement and calibration tools
  - Rapid prototyping tools
Software Debugging / Trace

- Allows developers to find and correct software issues
Software Debugging / Trace

- Typical bench set up for software debugging and trace
Measurement and Calibration

- Allows calibrators to adjust/tune calibration values (constants), and to measure key ECU parameters

ETAS XETK-V2

- Nexus Class 3+, JTAG, A/D Bus
- ETK I/F
- LEMO connector

ECU (Development Controller)

Developer’s PC

ethernet
Measurement and Calibration

- Typical set up in a development vehicle
Rapid Prototyping

- Allows developers to test new ideas and experiment without changing code in the ECU.
Rapid Prototyping

- Used in development vehicles and on benches
Presenter

- **Udo Zoettler** works at Lauterbach, Inc. and has been a Sales/Marketing Manager for the last 17 years. Udo's work is focused on sales and customer acquisition as well as providing training classes to end customers for Lauterbach debugger products used in automotive and embedded systems software development. Prior to Lauterbach, Inc., Udo held a sales/marketing manager position at Krohn & Stiller.

Udo received his MSE from the Technical University Ilmenau, Germany, in 1989.
ECU Software Debugging and Trace

Udo Zoettler, Lauterbach
TRACE32
PowerTrace II
2\textsuperscript{nd} Generation Debug Tools

for
Nexus Aurora HSTP Interface based
Microcontrollers (MPC57xx)
Real time debugging and trace analysis

- Embedded software in engine and transmission controllers needs to be tested and validated for performance, safety and quality assurance.
- The utilization of the NEXUS class3 debug interface on the microcontroller allows the Lauterbach debugger real time access to all cores to display source code and to have read/write access to data memory without interference with the cores‘ real time code execution.
- Today’s focus will be to demonstrate multi core debug and high speed serial trace features on 3 e200Z4 cores based on a freescale MPC5746M (McKinley) device.
PowerTrace II Real Time Trace and Debugger

- Gigabit Ethernet + USB host interfaces
- Support for Nexus Aurora HSTP
- Up to 4 lanes of high speed serial trace
- 6Gb/sec bandwidth per lane
- Up to 4 GByte trace memory
- Program execution and data r/w history trace
- Performance Analyzer
- Function Runtime Analysis
- Code Coverage Analysis
- Real Time System Performance Analysis
- History based Trace debugging: CTS
- Long Term Trace Recording through Streaming Mode
LA-7699: PowerDebug II

LA-7694: PowerTrace II 4GB

LA-3738: Debugger Bundle AUTO26

LA-3911: Pre Processor MPC57xx Nexus Aurora

LA-3871: Conv. Samtec40 HSTP + AUTO26 to Samtec34

Freescale Eval Board MPC5746M with JTAG14 and Nexus standard Samtec34 interfaces

Typical Debug Tool Setup
NEXUS class3 debugger

- Run control: Single Step, Run, Break, Breakpoints
- Source code listing
- Read/Write real time memory access
- Flash programming
- Real time Trace: Program execution, Data r/w history
- Advanced features: Function Runtime Analysis, Code Coverage Analysis, Performance Analysis, History based trace debugging
- Long Term Streaming Mode real time trace
Run control, Source code listing, r/w real time memory access
Switch to Lauterbach debugger demo
Steve Rosenthal is a senior software engineer at ETAS, where he has been involved in vehicle diagnostic solutions, M/C tool (INCA) development and integration, and Rapid Prototyping software (EHOOKS). Prior to joining ETAS, Steve worked at Hewlett-Packard for a number of years as a software engineer and consultant.

Steve received his BS degree in Mathematics/Computer Science from Lawrence Technological University, Southfield, MI in 1987.
M/C tool Demo
Bypass + e-hooks demo
Multi tool use case – M/C +
debugger/trace arbitration demo

Steve Rosenthal
Randy Dees

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He has worked in both Product Engineering and Application supporting 8- to 32-bit microprocessors, integrated circuits for telecommunications, and 32-bit microcontrollers. He has been working with Nexus-based MCUs since 1999 and has been either the co-chairman or the chairman of the IEEE-ISTO 5001 Nexus Consortium’s technical subcommittee since 2000.
Freescale’s latest Nexus debug based MCU’s

Nexus 5001
Qorivva Automotive MCU Roadmap

- **Gen 1**
  - **0.25/0.35 μm**
    - MPC566
    - MPC565
    - MPC564
    - MPC563
    - MPC555
    - MPC562
    - MPC561

- **Gen 2**
  - **130 nm**
    - MPC5566
    - MPC5554
    - MPC5567
    - MPC5565
    - MPC5561
    - MPC5534
    - MPC5510

- **Gen 3**
  - **90 nm**
    - MPC5676R
    - MPC567xF
    - MPC567xK
    - MPC566xG/E
    - MPC564xS
    - MPC564xL
    - MPC564xB/C
    - MPC564xA
    - MPC563xM
    - MPC560xS
    - MPC560xP
    - MPC560xE
    - MPC560xB/C/D

- **Gen 4**
  - **55 nm**
    - MPC5777M
    - MPC5777C
    - MPC5775K
    - MPC5746M
    - MPC574xG
    - MPC574xC
    - MPC574xP

**Timeline**:
- **1998**: 
  - MPC5510
  - *Not considered Qorivva devices.*
- **2003**: 
  - MPC566
  - MPC565
  - MPC564
  - MPC563
  - MPC555
  - MPC562
  - MPC561
- **2008**: 
  - MPC5566
  - MPC5554
  - MPC5567
  - MPC5565
  - MPC5561
  - MPC5534
  - MPC5510
- **2012**: 
  - MPC5676R
  - MPC567xF
  - MPC567xK
  - MPC566xG/E
  - MPC564xS
  - MPC564xL
  - MPC564xB/C
  - MPC564xA
  - MPC563xM
  - MPC560xS
  - MPC560xP
  - MPC560xE
  - MPC560xB/C/D
  - MPC5777M
  - MPC5777C
  - MPC5775K
  - MPC5746M
  - MPC574xG
  - MPC574xC
  - MPC574xP

**Notes**:
- MPC5777M and MPC5746R to be announced November 2013.
- Separate security module.
- Supports functional safety.
- eTPU timer system.
- GTM timer system.
- No timer system.
Key Functional Characteristics
- Two independent 200 MHz Power Architecture z4 computational cores
  - Single 200 MHz Power Architecture z4 in lockstep
- eDMA – 64 channels (w/ lockstep DMA)
- 4M Flash with ECC
- 320k total SRAM with ECC
  - 256k of system RAM (incl. 32k of standby RAM)
  - 64k of tightly coupled data RAM
- 3 ΣΔ ADC converters – 12 channels
- 4 SAR converters – 52 channels
- Cross Triggering Unit
- Ethernet (MII-lite/RMII)
- DSPI – 7 channels (2 supporting µSec channel)
- LINFlex - 6 channels (2 supporting µSec channel)
- FlexCAN – 4 chls, 2 w/ flexible data rate capability
- SENT – 6 channels
- 2 eTPU2+ timers – 64 channels
- 1 eMIOS – 32 channels
- Reaction module – 10 channels

Key Electrical Characteristics
- -40 to +125 °C (ambient)
- Single 5V power supply

Package
- 176 LQFP, 252 MAPBGA
- 292 MAPBGA eCal package (incl. RAM buddy chip) for emulation/debug

Enablement
- Software : AutoSAR drivers
- Tools : Debugger (Lauterbach), multicore compiler (Wind River and Green Hills)
**Cores & Memory**
- Two independent 27 dual issue computational cores @ 264MHz
  - Cores include VLE, SPE1.1, FPU, MMU
  - 16kB i-cache & 16kB data-cache w/coherency
- Single 27 lockstep core @ 264MHz (for ISO26262 and ASIL-D)
- Up to 8.25MB Flash RWW w/ECC including 4 x 64kB EEPROM
- Up to 589kB total SRAM
  - 512kB on-chip static RAM w/ECC (up to 48KB standby)
  - 45kB eTPU RAM, 32kB data cache (w/line locking)
- Security
  - PASS and TDM (Tamper Detection)
  - CSE2 (Crypto Services Engine for Encryption & Secure Boot)

**I/O & System**
- Up to 70ch eQADC from 4 converters w/12bit resolution
  - On-chip temperature sensor and VGA (x1,x2,x4)
  - 12 x Decimation Filters w/hardware knock integrators
  - Timers – up to 128 channels (96ch eTPU2+ and 32ch eMIOS)
  - 2 x 64ch eDMA support (128ch total)
  - 6 x CAN ports (4 x FlexCAN + 2 x MCAN with Flexible Datarate)
  - Ethernet
  - DSPI – 5 channels (2 supporting μSec ch.)
  - eSCI – 6 channels (2 supporting μSec ch.)
  - Reaction module – 8 channels for current control
  - Up to 12ch SENT, Zipwire, 2ch PSI-5
  - 1 x CRC unit – w/ 3 independent channels,
  - 4 x protected port outputs, MPU and MMU
  - FMPLL + PLL
  - Safety Monitors – e2eECC, CLK, Voltage, Fault Collection

**Packaging & Enablement**
- 416 PBGA, 516 PBGA
- Calibration – VertiCal (using 552CSP)

**Optional Content:**
- 300MHz per core
- 4 x Sigma Delta ADCs (up to 20ch, 16bit)
MPC5777M 8M Block Diagram

Key Functional Characteristics

- Two independent 300 MHz Power Architecture z7 computational cores
  - Single 300 MHz Power Architecture z7 core in delayed lockstep for ASIL-D safety
- Single I/O 200 MHz Power Architecture z4 core
- eDMA controller – 128 channels
- 8M Flash with ECC
- 596k total SRAM with ECC
  - 404k of system RAM (incls. 64k standby)
  - 192k of tightly coupled data RAM
- 10 ΣΔ & 12 SAR converters – 84 channels
- Ethernet (MII/RMII)
- DSPI – 8 channels (3 supporting µSec ch.)
- LINFlex - 6 channels (3 supporting µSec ch.)
- MCAN-FD/TTCAN – 4x modules/1x module
- GTM – 248 timer channels

Key Electrical Characteristics

- -40 to +125 °C (ambient)
- 165 °C junction for KGD
- 1.26V Vdd, 5.0V I/O, 5V ADC

Package

- 292 PBGA, 416 PBGA, 512 PBGA
- eCal emulation device for each package

Enablement

- Software: AutoSAR drivers
- Tools
  - Debugger: Green Hills, Lauterbach and PLS
  - Multicore compiler: HighTec, GCC, Wind River & Green Hills
  - Simulation tools
Key Functional Characteristics
- Two independent 200 MHz Power Architecture z4 computational cores
  - Single 200 MHz Power Architecture z4 core in delayed lockstep for ASIL-D safety
  - Single I/O 200 MHz Power Architecture z4 core
- eDMA controller – 64 channels
- 4M Flash with ECC
- 320k total SRAM with ECC
  - 128k of system RAM (incl. 64k standby on 292 PBGA package)
  - 192k of tightly coupled data RAM
- 6 ΣΔ & 8 SAR converters – 60 channels on 292 MAPBGA, 48 channels on 176 LQFP
- Ethernet (MII/RMII)
- DSPI – 7 channels (2 supporting µSec ch.)
- LINFlex - 5 channels (2 supporting µSec ch.)
- MCAN-FD/TTCAN – 3x modules/1x module
- GTM – 120 timer channels

Key Electrical Characteristics
- -40 to +125 °C (ambient)
- 165 °C junction for KGD
- 1.26V Vdd, 5.0V I/O, 5V ADC

Package
- 176 LQFP / EP, 292 PBGA
- eCal emulation device for each package

Enablement
- Software: AutoSAR drivers
- Tools
  - Debugger: Green Hills, Lauterbach and PLS
  - Multicore compiler: HighTec, GCC, Wind River, GHS
  - Simulation tools
**Core**
- Dual up to 200 MHz Power™ ISA e200 core (e200z420)
- 32 bit Reg File, 64 bit BIU with E2E ECC,
- 64kB RAM of D-LMEM with MPU for fast context switch + local data
- 8KB 2-way I-cache / 4KB 2-way D-Cache
- 1x Scalar FPU (compiler supported) per core
- Safety enhanced Cores – VLE only
- No Signal processing unit extension + NO MMU
- Delayed Lock Step configuration only

**Memory**
- 2.5 MBytes NVM with ECC (with add. Safety measure for address).
- 64kB EEE (Data Flash) available incl. ECC
- Up to 384 Kbyte global system SRAM with ECC (Addr + Data)

**I/O**
- 3 x FlexCAN (64+2x32 message buffers)
- 1 x FlexRay (Dual Channel 64 msg. buffers)
- 2 x LINFlex (Uart/Lin protocol driver)
- 4 x DSPI (4 cs each)
- 2x FlexPWM (2x 12ch for 2 independent Motors Controlled)
- 3 x eTimer modules (18 channel total)
- 4 x SAR ADC – 1MS/s target 5V input capable
- 2 x Cross-triggering unit for motor control automatism
- 2x SENT
- Ethernet (257BGA only)

**System**
- Interprocessor I/F SIPI (~ approx 300Mbaud)
- Safe DMA
- Fault Collection unit, WDG, T-sens, & CRC computing unit
- Nexus debug interface – Aurora
- Dual-PLL (Peripheral + System Core)
- 3.3 V Single supply: internal regulator with external power stage or External supply
- 3.3 V I/Os (ADC 5 V capable)
- 144 LQFP / 257 MAPBGA 0.8 mm pitch
- Tj = 150°C
**MPC5748C/G Block Diagram**

**Applications:**
- High end Gateway and Body Modules

**Key Characteristics:**
- 2x e200z4 + 1x z2 cores, FPU on z4 cores
- 160 MHz max for z4s and 80 MHz on z2
- HSM Security Module option supports both SHE and EVITA low/medium standard
- Media Local Bus supports MOST communication
- 2 x USB 2.0 (1 OTG and 1 Host module) support interfacing to 3G modem and infotainment domain
- 2 x Ethernet 10/100 Mbps RMII, MII, +1588, AVB
- CAN module optionally supports CAN FD
- SDHC provides standard SDIO interface
- Low Power Unit provides reduced CAN, LIN, SPI, ADC functionality in low power mode
- Designed to ISO26262 process for use in ASIL B
- -40 to +125°C (ambient)
- 3.0V to 5.5V

**Packages:**
- 176 LQFP, 256 BGA, 324 BGA

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**Features available depend on package and device version**
**MPC577xK 4M Block Diagram**

**Specifications:**
- **CPU:** 3x PPC: 2x e200z7 266 MHz Power dual issue with SPE2 and VFPUs and e200z4 133MHz in permanent lockstep
- **SPT:** FFT Accelerator, DMA
- **Analog:** Octal SD + 4 SAR, Ultra low jitter PLL, precision DAC
- **Package:** 356 PBGA – 0.8 mm pitch – 17 x 17 mm² body
- **Temp Range (Ta):** -40 to 125°C, 150 °C Tj, AEC-Q100 Grade 1
- **Main Supply:** 3.3V IO (5V SAR) and 1.2V Core (ext or PMU)

**Key Features:**
- **Safety:** developed as per ISO26262 with target ASIL-D
- **Safety Enablement:** Safety Manual and FMEDA
- **SPT:** Radix4/2, r2c, c2c, 50 MHz 16 bit twiddle, 24 bit results
- **SRAM:** Multi ported SRAM Ctrl and 1.5MB SRAM with ECC
- **Top of Class Analogue IP:** PLL, DAC, OSC and ΣΔ ADC
- **SW Enablement:** QMS MCAL and/or Safe Mcal Asil B (D)

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**Diagram Details**
- **ADC Input:** 8 x ΣΔ – 10MHz
- **DAC:** 2Ms/s 8 bit DAC
- **SPT:** FFT Accelerator, DMA
- **Analog:** Octal SD + 4 SAR, Ultra low jitter PLL, precision DAC
- **Package:** 356 PBGA – 0.8 mm pitch – 17 x 17 mm² body
- **Temp Range (Ta):** -40 to 125°C, 150 °C Tj, AEC-Q100 Grade 1
- **Main Supply:** 3.3V IO (5V SAR) and 1.2V Core (ext or PMU)
Questions and Answers

Any questions that we are unable to accommodate due to time constraints will be answered on the website www.nexus5001.org
Thank You!

For more information on Nexus 5001 Forum, please visit:

www.nexus5001.org

For questions or comments email admin@nexus5001.org