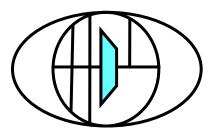
## IEEE 5001/Nexus-2010 integration with 1149.7

#### Neal Stollon neals@hdldynamics.com



HDL Dynamics SoC Solutions



#### **IEEE 5001 Nexus Introduction**

- Real Time Debug Instrumentation Architecture and methodology standard
  - IEEE Standard 5001 ISTO program 20+ member companies
  - CPU/SoC architecture agnostic standard (15 different architectures to date)
  - Default standard use in US Automotive electronics
  - Aligned with other standards bodies 1149.1. 1149.7, Power.org, OCP-IP
  - Nexus Specification is freely available www.nexus5001.org
  - Nexus 5001-20010 specs in work include support for 1149.7 interfaces
  - Support from range of vendors in the tools community
- Nexus provides a Instrumentation toolbox for SoC Debug
  - Debug oriented packet messaging (TCODES) and application registers
  - 4 levels of increasing debug functionality
    - Embedded run control, Breakpoints , Instruction/data trace
    - Memory and Register configuration and system analysis access
  - Defines Multiple Trace and Debug Access Methods and interfaces
    - JTAG & Parallel– AUX. Read (Trace) / Write (Configuration) Ports
    - High speed Serdes and 1149.7 2010 standard



#### **REFERENCE - Nexus Members**

Nexus Membership - 2009



DEVELOPMENT TOOLS



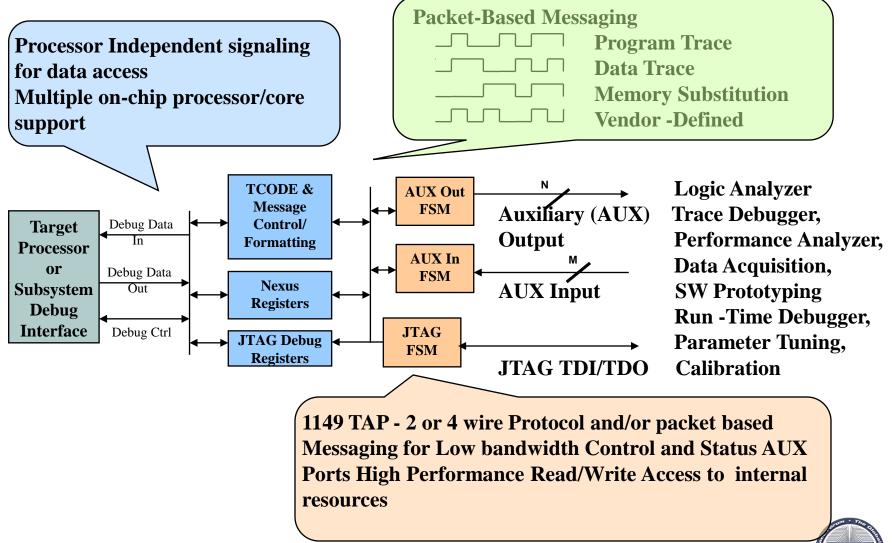




Engineering Tools



#### 5001 Nexus Debug Environment





INOLOGY ORGANIZATION

#### Nexus packet TCODE messages

- Nexus Messages consist of 6 bit TCODE (Transfer Code) followed by message specific number of packets
- Packet may be
  - Fixed constant size as defined by spec
  - Variable min (1 bit) value required
  - Vendor Fixed- constant size per target
  - Vendor variable variable size /message
- Messages can be Sync or Non-sync
  - Sync message include full address
  - Non-Sync include only relative change
- •Each message contains a source packet
  - Indicates source IP block of message
  - Allows simple Multi-core Nexus support on per message basis
- •Each message contains optional timestamp

Program Trace - Indirect Branch Message			Direction: from target			
Minimum Packet Size (bits)	Packet Name	Packet Type	Description			
0	TSTAMP	Vendor-variable	Number of cycles message was held in the buffer or the full timestamp value. For targets that do not implement timestamping (or use pins for timestamping), this field may be omit- ted. Refer to <b>4.11.2 - Timestamping via AUX</b> .			
1	U-ADDR	Variable	The unique portion of the branch target address for a taken indirect branch or exception.			
1	I-CNT	Variable	Number of instruction units executed since the last taken branch.			
0	B-TYPE	Vendor-fixed	Branch type. For targets that do not need to dif- ferentiate branch types, this packet can be omit- ted (see <b>Table 5-8</b> ).			
0	SRC	Vendor-fixed	Client that is source of message. For targets with only a single client, this packet can be omitted.			
6	TCODE	Fixed	Value = 4			

Fixed and variable packets required for minimum packet definition Vendor packets are where target differentiation/value is added



## Nexus access under JTAG

IR Nexus\_Enable command DR Nexus Reserved Register Select DR Nexus Message to IPMR register parse message in register DR Nexus Message to OPMR register scan out data in register

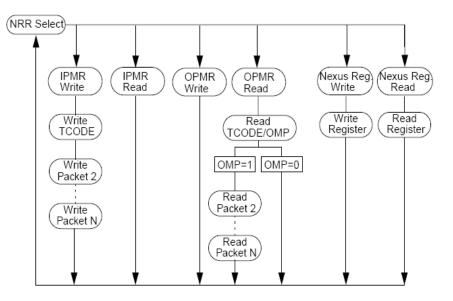
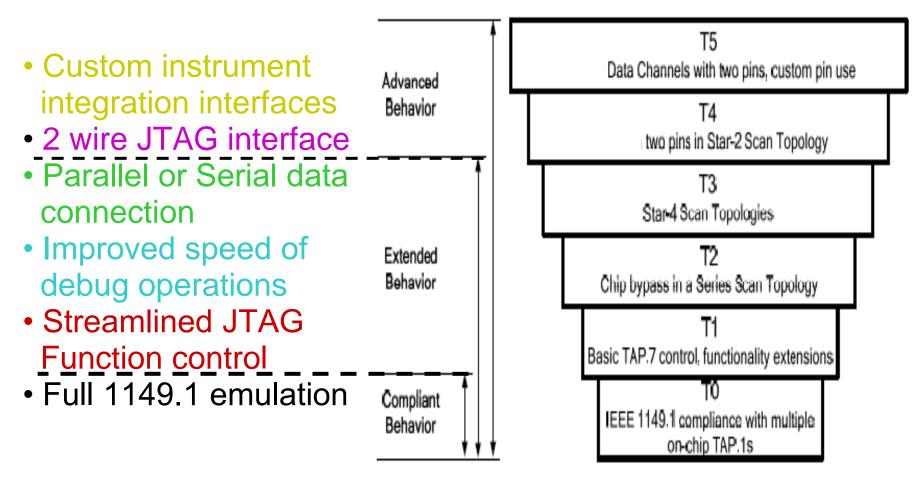


Figure 9-4 IEEE 1149.1 Controller State Diagram for Public Messaging



#### 5001 Nexus integrates IEEE 1149.7 for Next Generation JTAG



Increasing layers of functional enhancements Based on compliance with 1149.1 operations



#### 1149.7 Feature List

<u> </u>			i			
Extended - Operation within Star-4 Topology						T5
Directly addressable, TCA and CIDs						
Star-4 Drive Conflict Prevention					- 4	
Series/Star Scan Equivalence (SSDs)					14	
Extended Series Performance						
Coupling/Decoupling of STL						
Start-up With STL Decoupled						
Extended - Optional Functions						
TAP.7 Power Control						
Test Reset Generation						
Functional Reset Request				T3		
Extended - Control Levels						
Control Level Two – Cmds. and Regs.			T2			
Control Level Three Reserved.		T1				
Control Level Four/Five Scan Paths						
Control Level Six and Seven DTS Use						
1149.1 Compliance						
IEEE 1149.1 compliance at start-up	<b>_</b>					
Multiple Embedded TAPs	<b>T</b> 0					
Coupling/Decoupling of Embedded TAPs:						
Inclusion and exclusion of DR Scan Paths						

Advanced - Data Channels			
Data Channel 1			
Data Channel 0			
No Data Channels, don't go offline			
BDX/CDX Transfers			
Advanced - Operation within Star-2 Topology			
One of Four Start-up Options			
Compatibility between different feature sets			
TS or DTS Clock Source			
Test reset equivalent Escape Sequence			
Star-2 Drive Conflict Prevention			
2/4 pin (With or without TIDC/TDOC pins)			
Programmable function TDIC/TDOC pins			
Scan Formats:			
– Minimal Number are Mandatory			
– Very Optimized for Debug			
– Optimized for Debug			
– Optimized for Test			
– Optimized for Non-Compliant IP			
Extended - Operation within Star-4 Topology			T5



# Key points

- This has historically allowed different access mechanisms
  JTAG and Parallel Aux ports under a common framework
- Nexus-2010 adds new access port support
  - SERDES (Aurora protocol)
    - Can be treated as very fast AUX port
  - 1149.7
    - Nexus Message can be treated as just another register be read/written
    - Changes to FSM per 1149.7 are local to the Port Implementation



## **Open Debug Interconnect model**

Implementation Layer	Typical Tasks	Location
1. Physical Port Layer	JTAG/Nexus TAP IO, chain and debug block wires JTAG/Nexus TAP FSM (connection level)	Target
2. Data Control Layer	Debug IP specific Commands/Registers/FSM User defined JTAG/NEXUS debug instructions Extended/Optional Debug block registers	Target
3. Debug Driver Layer	Debugger Protocol, clocking (probe specific API)	Probe
4. Data Transport Layer	APIs debug command sets, run control API	Host PC
5. Session Control Layer	Device connection setup & parameters, Remote debug server ex. GDBserver,	Host/PC
6. Debug GUI Layer	Debugger UI, GDB commands, trace viewers Set/observe watch/break/trace points, event trigge In-the-loop Run control - go/halt/single step	Host/PC ers,
7. Application Layer	Eclipse, other IDE, Global (Multi-tool) data management	Host/PC

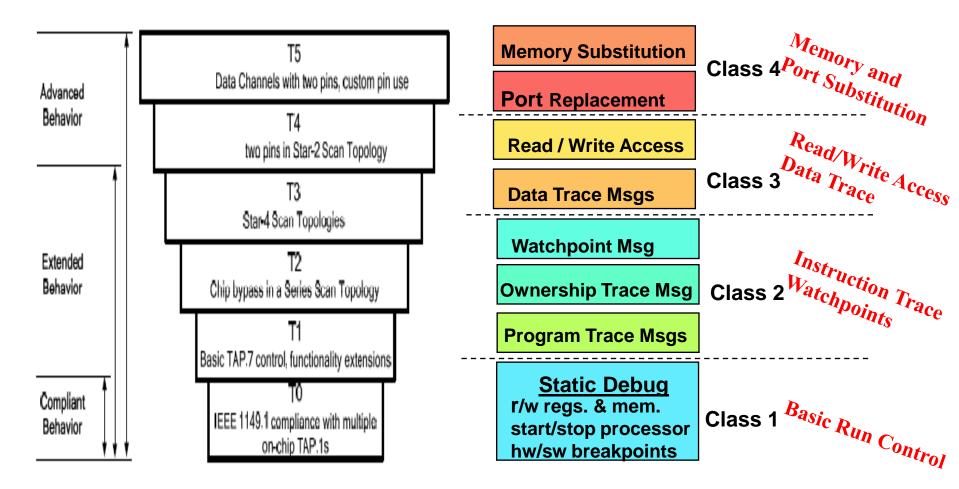


## **Open Debug Interconnect model**

Implementation Layer	Typical Tasks		Location
1. Physical Port Layer	hysical Port Layer JTAG/Nexus TAP IO, chain and debug block wires JTAG/Nexus TAP FSM (connection level)		Target
	1149.7 interface fits in here		
2. Data Control Layer	Target		
	Nexus TCODE architecture fit	s in here	
3. Debug Driver Layer	Debugger Protocol, clocking	Probe	
	Debug tools however will nee	ed to support both	



### **Nexus Feature Classes**



No direct correlation between 1149.7 T Classes and Nexus Classes



## 1149.7 BDX/CDX

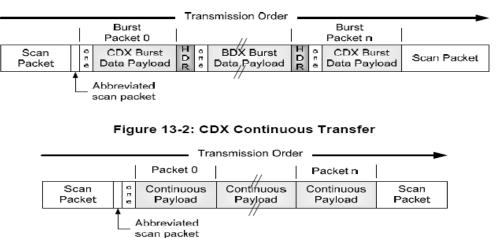
Directly addressable, TCA and CIDsImage: Property of the property of							
Directly addressable, TCA and CIDsImage: Property of the property of	Extended - Operation within Star-4 Topology						T5
Series/Star Scan Equivalence (SSDs)Image: Component of the system of the sy	Directly addressable, TCA and CIDs						
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Test Reset GenerationImage: Control Level Sector Control Level Sector Control Level Two - Cmds. and Regs.T3Control Level Two - Cmds. and Regs.Image: Control Level Three Reserved.Image: Control Level Four/Five Scan PathsImage: Control Level Six and Seven DTS UseImage: Control	Extended - Optional Functions						
Functional Reset RequestT3Extended - Control LevelsImage: Control Level Two - Cmds. and Regs.T2Control Level Two - Cmds. and Regs.T1Control Level Three Reserved.T1Control Level Four/Five Scan PathsImage: Control Level Six and Seven DTS UseControl Level Six and Seven DTS UseImage: Control Level Six and Seven DTS Use1149.1 ComplianceImage: Control Level TAPsMultiple Embedded TAPsT0Coupling/Decoupling of Embedded TAPs:Image: Control Level Six and Seven DTS Use	TAP.7 Power Control						
Extended - Control Levels    Image: Control Level Two - Cmds. and Regs.    T2      Control Level Two - Cmds. and Regs.    T1      Control Level Three Reserved.    T1      Control Level Four/Five Scan Paths    T1      Control Level Six and Seven DTS Use    Image: Control Level Six and Seven DTS Use      1149.1 Compliance    T0      IEEE 1149.1 compliance at start-up    T0      Multiple Embedded TAPs    T0	Test Reset Generation						
Control Level Two - Cmds. and Regs.T2Control Level Three Reserved.T1Control Level Four/Five Scan PathsT1Control Level Six and Seven DTS Use1149.1 ComplianceIEEE 1149.1 compliance at start-upT0Multiple Embedded TAPsT0Coupling/Decoupling of Embedded TAPs:I	Functional Reset Request				T3		
Control Level Three Reserved.  T1    Control Level Four/Five Scan Paths  Image: Control Level Six and Seven DTS Use    Control Level Six and Seven DTS Use  Image: Control Level Six and Seven DTS Use    1149.1 Compliance  Image: Control Level Six and Seven DTS Use    IEEE 1149.1 compliance at start-up  T0    Multiple Embedded TAPs  T0	Extended - Control Levels						
Control Level Four/Five Scan Paths    Image: Control Level Six and Seven DTS Use      1149.1 Compliance    Image: Control Level Six and Seven DTS Use      IEEE 1149.1 compliance at start-up    Image: Control Level Six and Seven DTS Use      Multiple Embedded TAPs    TO      Coupling/Decoupling of Embedded TAPs:    Image: Control Level Six and Seven DTS Use	Control Level Two – Cmds. and Regs.			T2			
Control Level Six and Seven DTS Use    1149.1 Compliance    IEEE 1149.1 compliance at start-up    Multiple Embedded TAPs    Coupling/Decoupling of Embedded TAPs:	Control Level Three Reserved.		T1				
1149.1 Compliance    IEEE 1149.1 compliance at start-up    Multiple Embedded TAPs    Coupling/Decoupling of Embedded TAPs:	Control Level Four/Five Scan Paths						
IEEE 1149.1 compliance at start-up    Multiple Embedded TAPs    Coupling/Decoupling of Embedded TAPs:	Control Level Six and Seven DTS Use						
Multiple Embedded TAPs <b>TO</b> Coupling/Decoupling of Embedded TAPs:	1149.1 Compliance						
Coupling/Decoupling of Embedded TAPs:	IEEE 1149.1 compliance at start-up						
	Multiple Embedded TAPs	T0					
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– Optimized for Non-Compliant IP			
Extended - Operation within Star-4 Topology			Т5
Extended - Operation within Star-4 Topology		 -	115



## CDX /BDX

- Background Data Transport (BDX) utilize idle bandwidth during TAP IDLE, PAUSE\_DR, and PAUSE\_IR for transfers
  - Interesting for improving throughput of data intensive trace/calibration operations
- Custom Data Transport (CDX) implement a custom link protocol to "on the fly" change direction of the data transfers.
  - Interesting since majority of Nexus data intensive transfers are driven from target



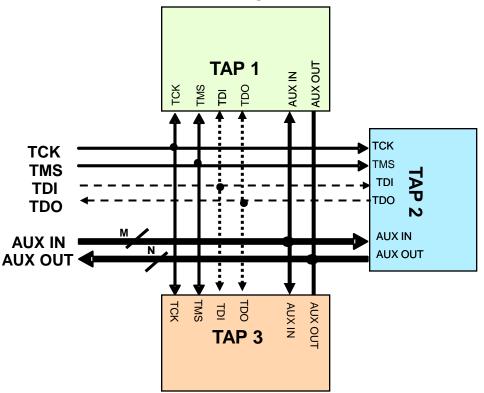




#### IEEE 1149.7 JTAG & 5001 Nexus

- Nexus debug over 2 wire interface as required
- Does not impact Nexus TCODE protocol or Multi-Processor/SoC debug support
- Nexus Aux In and Out ports extend 1149.7 bandwidth options for trace, calibration, mem access, ...
- 1149.7 Star configurations allow direct control/data connection for Nexus ports in different devices
  - Address cases where synch is needed with AUX ports
- Nexus operation is compatible with 1149.7 (T0-T5) classes
  - Nexus protocol sits on top of 1149.7 signaling,
  - Potential improved performance using 1149.7 T5 CDX/BDX functions





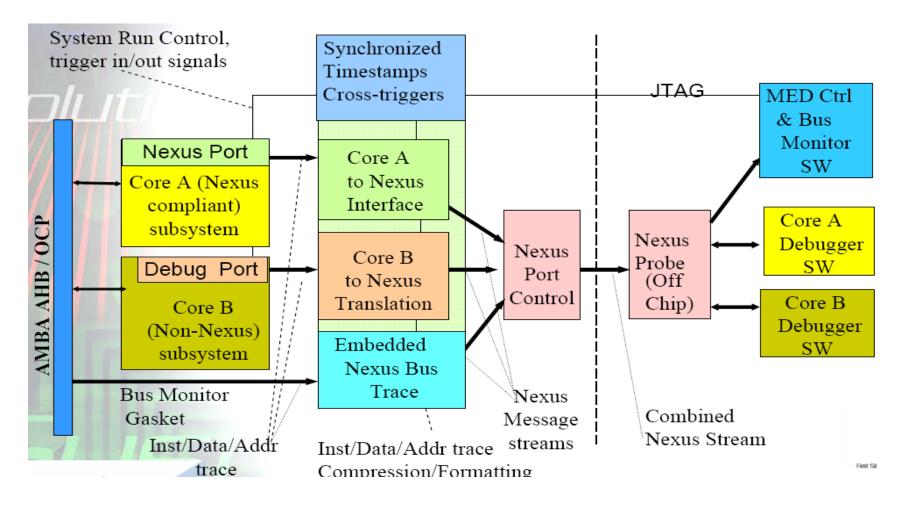


### THANK YOU

#### NEXUS 2010 SPECIFICATON SHOULD RELEASE IN 4Q2010



## **REFERENCE - Nexus Example**





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