The Engine of SOC Design

TRAX: A Nexus 5001-compatible Real-time Trace Tool for SoC Debug

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Introduction

- **Tensilica's processors**
  - Xtensa – configurable and extensible
  - Diamond standard cores
  - http://www.tensilica.com/ for more details
- **… are extensively used in complex SoCs**
  - multiple heterogenous processor core systems
  - running sophisticated software
  - with many HW and SW interactions
- **Debug is vital**
  - we already provide the traditional run-control debug
  - debugger ➔ JTAG ➔ OCD (on-chip debug) HW of core

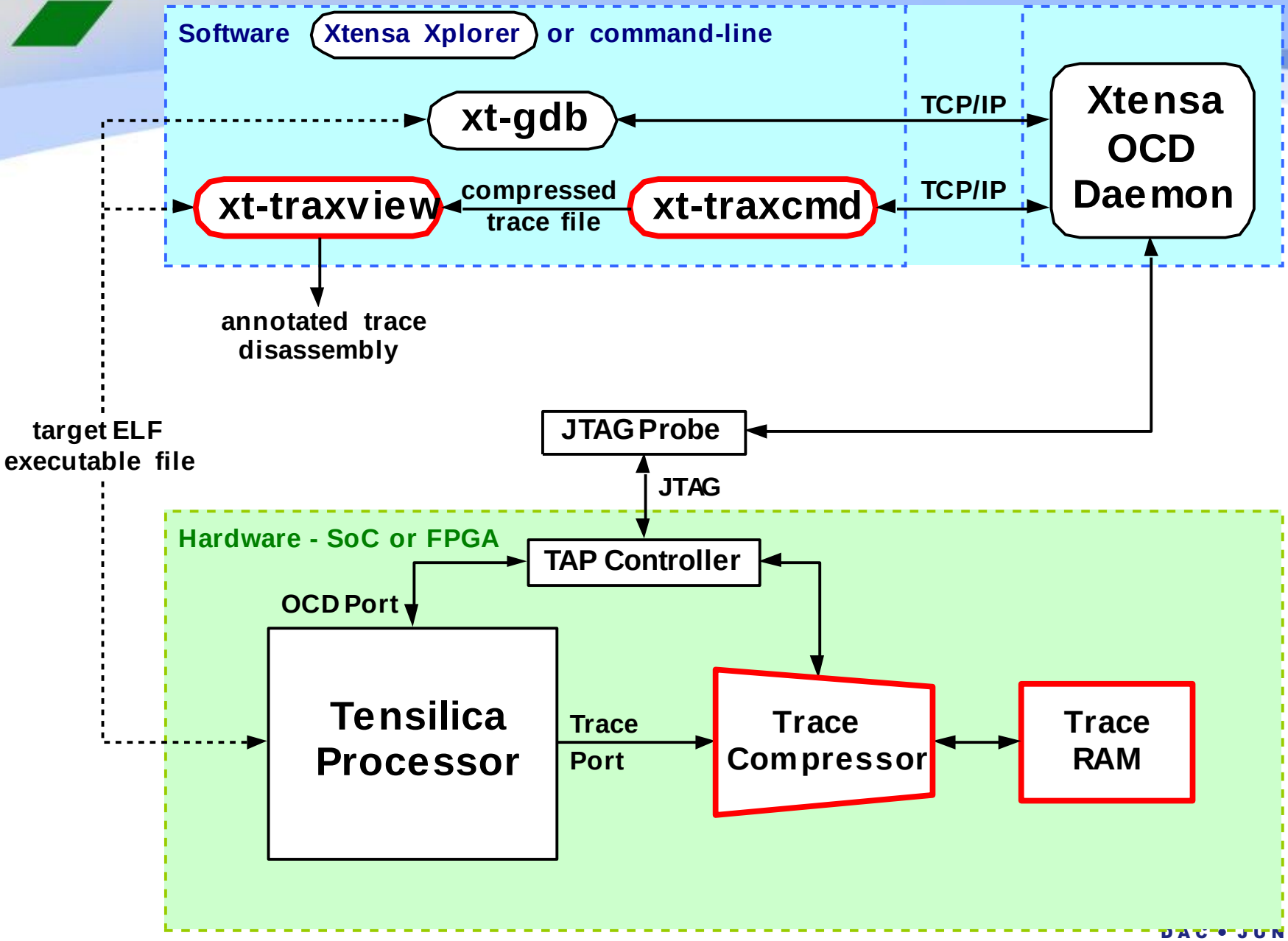
Escalating Debug Challenges

- **Non-intrusive debug**
  - real-time visibility
- **Debug of the deployed system**
  - small footprint
- **How did I get here?**
  - cause of bug distant from detection
- **Multi-core systems**
  - interactions between multiple processors
- **Chip pins are limited**

Real-time Trace

- **Real-time trace addresses these issues**
- **How to implement for Xtensa processors ?**
  - roll our own ? …pick existing standard ?
- **Nexus 5001 Forum Standard**
  - debug and trace well considered
  - existing third-party HW and SW ecosystem
  - excellent compression of trace possible
  - forum quite open to feedback of improvements
- **Tensilica's real-time trace product – TRAX**
  - TRace Analyzer for Xtensa

TRAX Overview



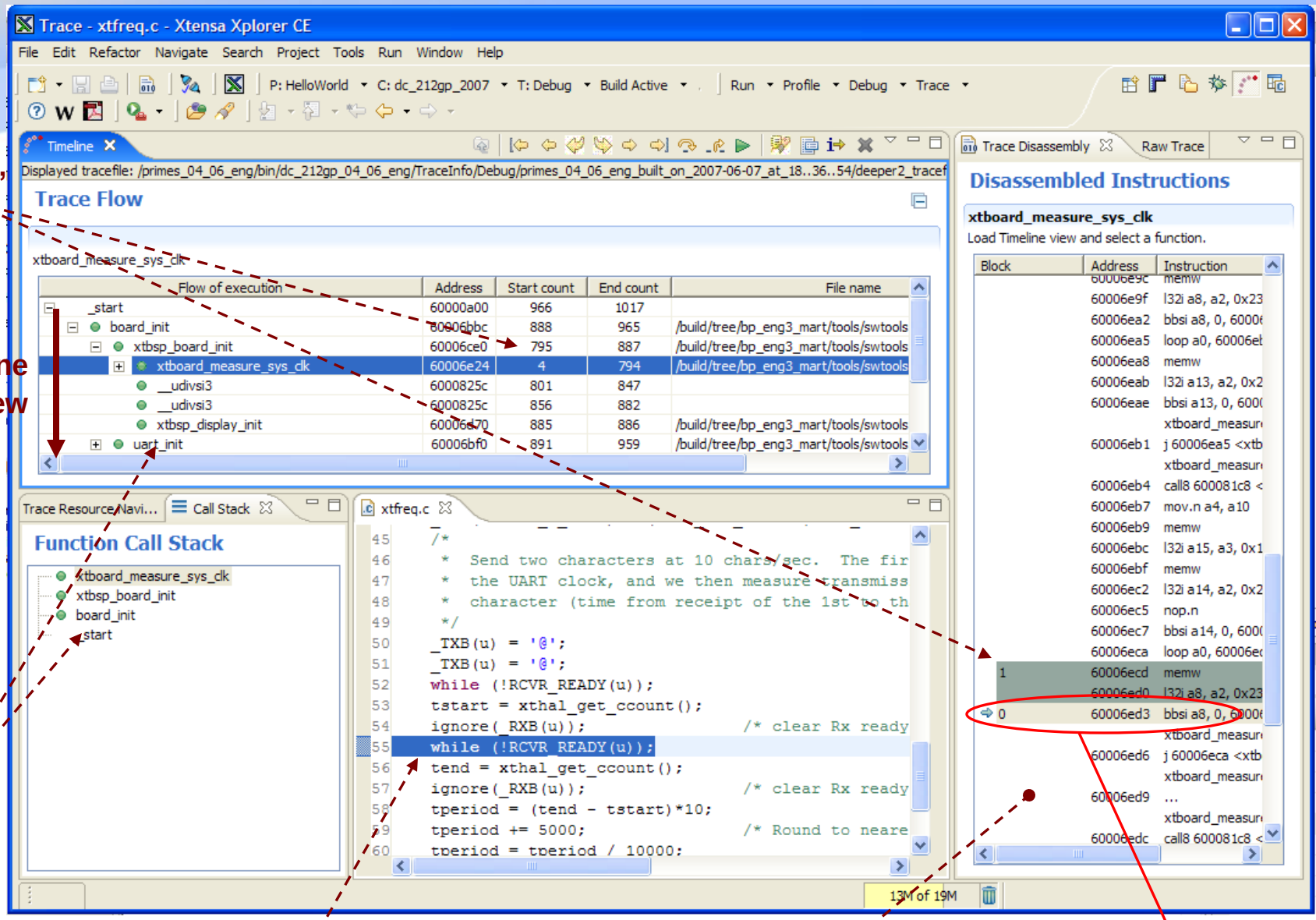
Key Features of TRAX

- **Nexus 5001 compatible**
- **On-chip trace**
  - addresses bandwidth and pin-count challenges
- **Traces program flow only**
- **Provides good compression**
  - less than one bit of trace data per instruction executed
- **Small area**
  - TraceCompressor less than 10K gates
  - 4KB of TraceRAM covers the majority of debug needs
- **PC-based triggering**
- **Multi-core support and cross-triggering**

Nexus Implementation Choices

- **Small subset of Nexus messages (four)**
  - only traditional branch messages
  - sync message for resource-full conditions
- **All branches treated as indirect**
  - allows backwards decompression of trace
  - takes away the need for periodic sync messages
- **8-bit AUX port width**
  - 2 bits for control (MSEO) and 6 bits for payload (MDO)
  - 32-bit rd/wr interface to TraceRAM – four parallel AUX ports
- **Buffer in TraceCompressor ensures no overflow**
- **Nexus Recommended Registers**
  - did not fit with existing debug mechanisms
  - did use Nexus FSM for accessing registers

Integrated Trace Display



Code 'block' Number

Timeline View

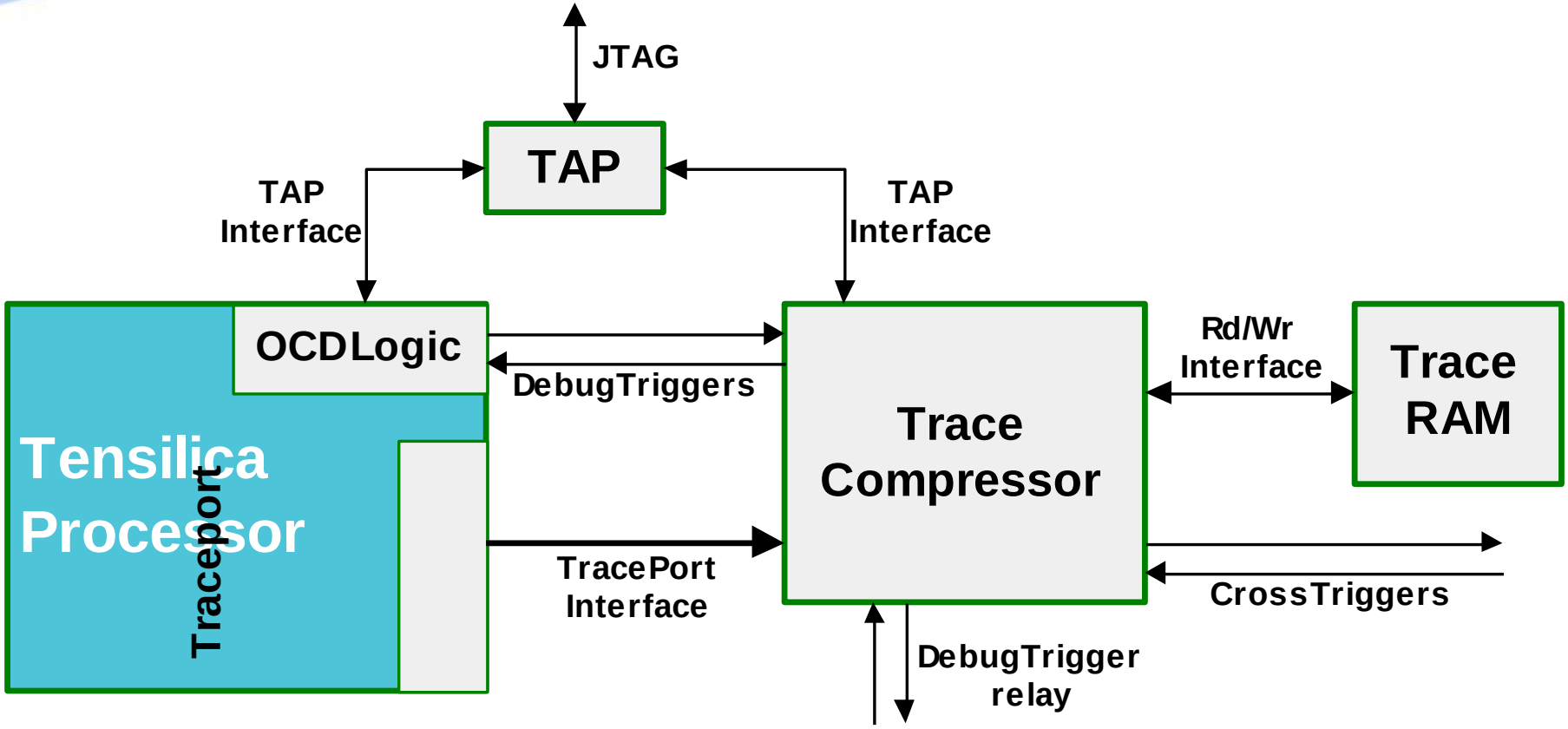
Trace Execution Stack

Application Code Traced

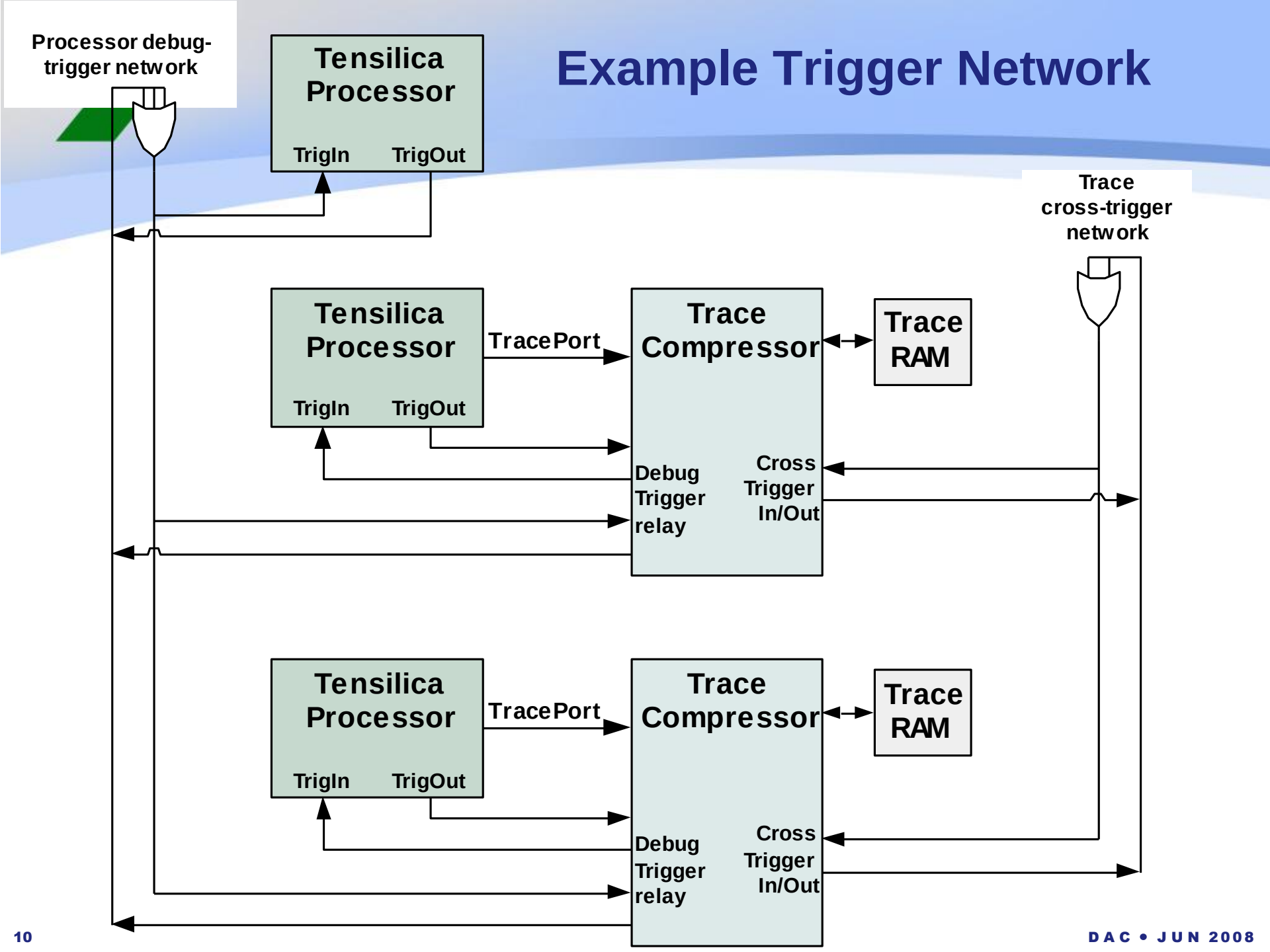
Trace Disassembly Window

PC Trigger !!

TRAX Hardware Components



Example Trigger Network

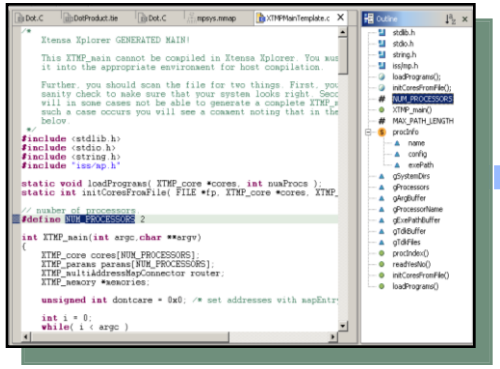


Summary

- **Small and simple trace solution**
- **First generation trace product**
  - main focus was on light footprint solution
  - we will grow the product based on user feedback
- **Thank you for your attention !!**

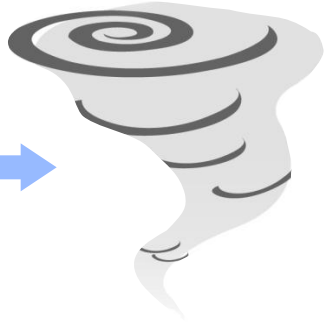
Supplementary Slides

Automatic Generation of Application-Specific Embedded Processors



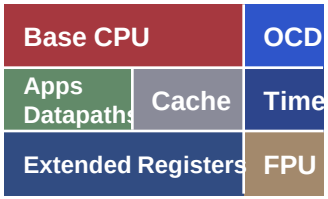
Processor configuration

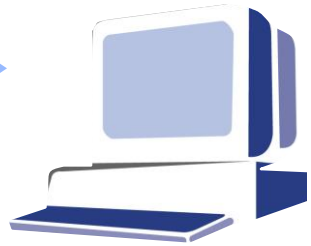
1. Select from menu of config options
2. Automatic instruction discovery (XPRES Compiler)
3. Explicit instruction description (TIE)



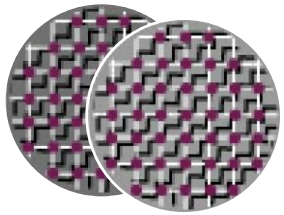
Tensilica Processor Generator

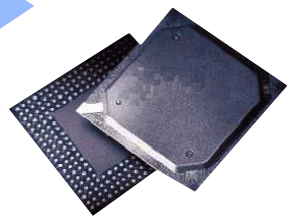
Application-optimized processor implementation (RTL)





Tailored SW Tools: Compiler, debugger, simulators, OS ports





Build with any process in any fab

Design processor with full SW toolchain in one hour

TraceCompressor

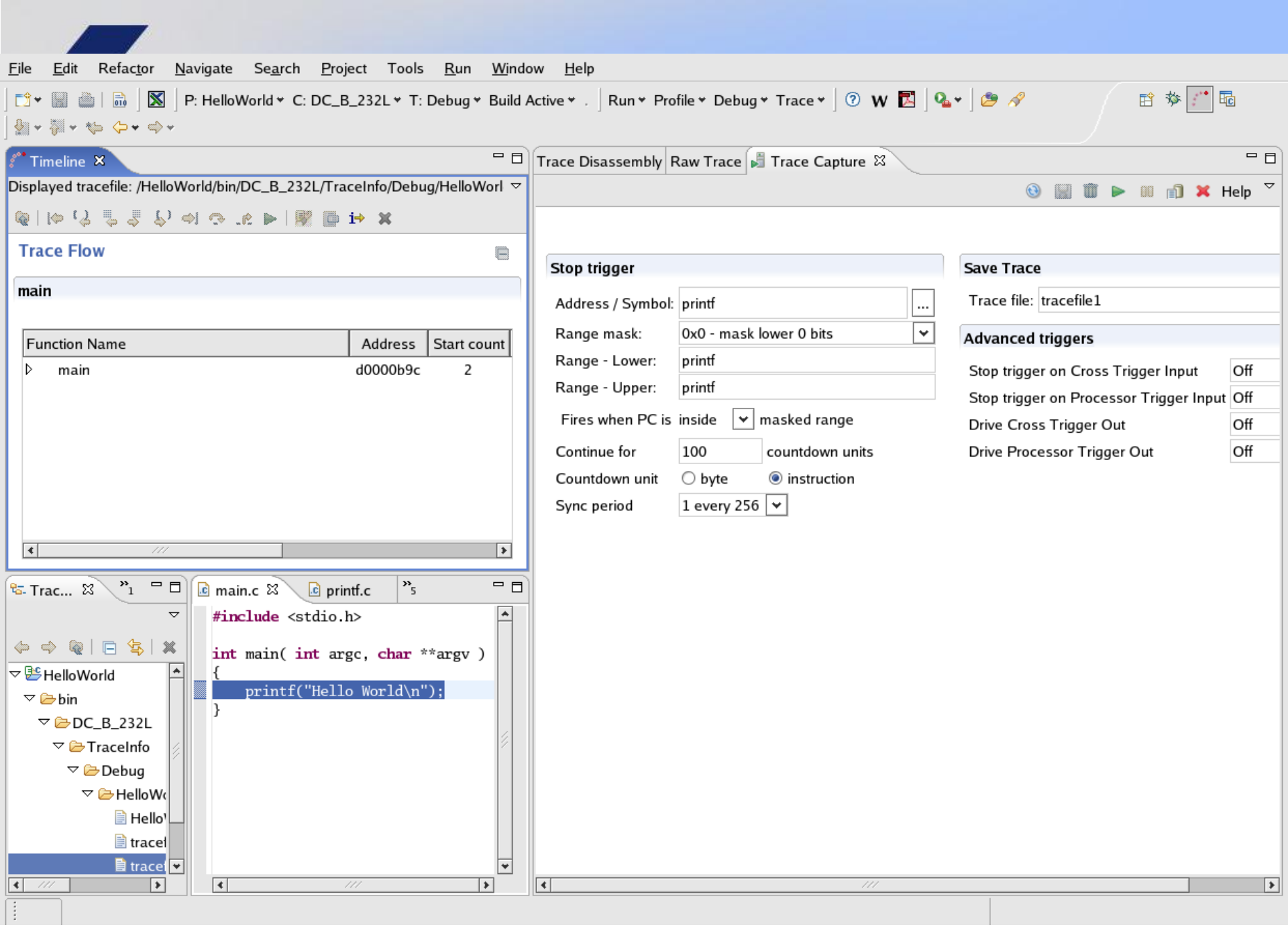
- **Receives PC and CTI/exception/interrrupts/etc info from TracePort**
- **Creates Nexus messages**

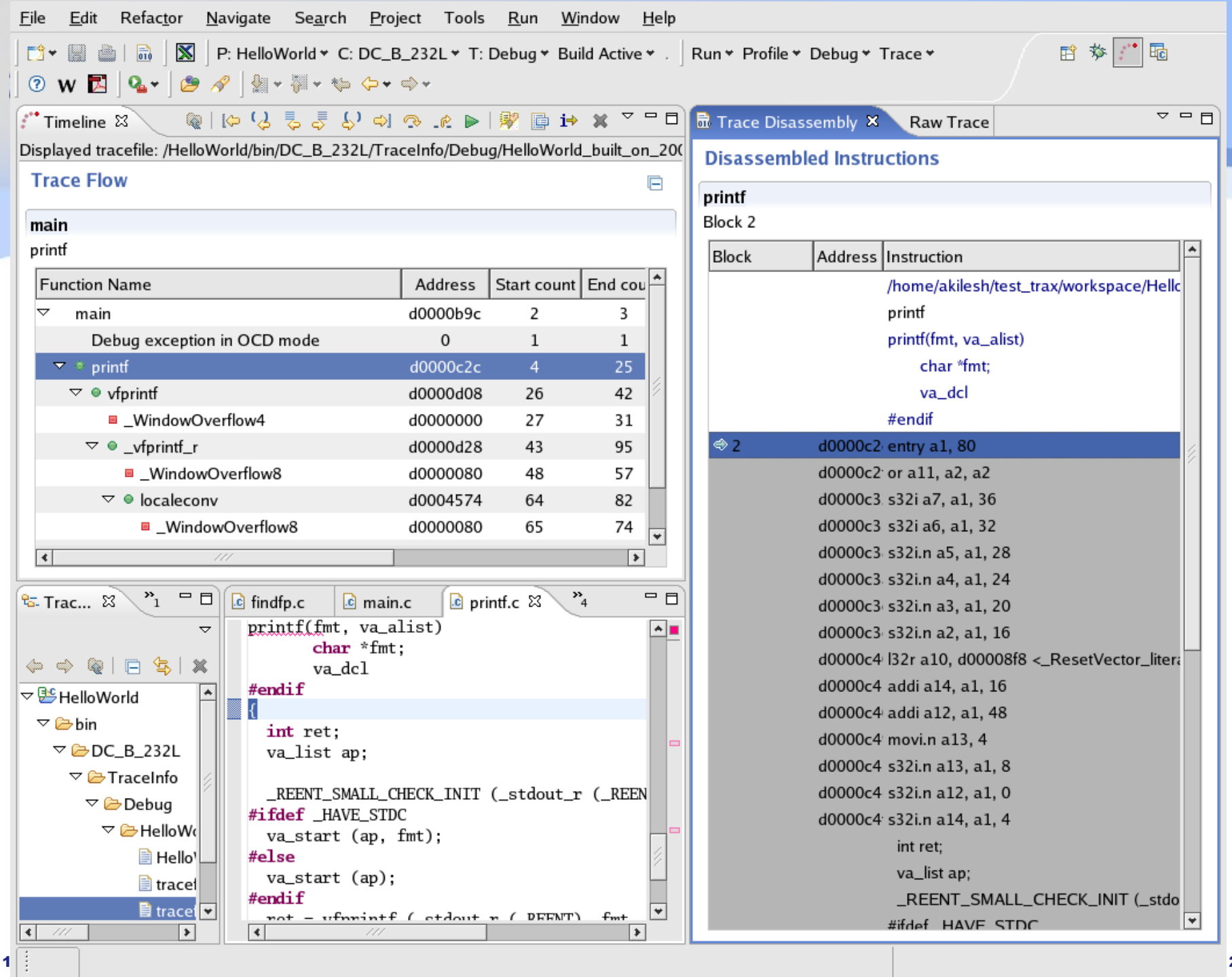
Message	Variable field	Variable field	Fixed field	Fixed field	Fixed field
Branch	U-ADDR	I-CNT	B-TYPE	-	TCODE
Br w Sync	F-ADDR	I-CNT	B-TYPE	DCONT	TCODE
Sync	PC	I-CNT	-	DCONT	TCODE
Correlate	-	I-CNT	EVCODE	-	TCODE

- **To 8-bit AUX port width**
  - 2 bits for control (MSEO), 6 bits for payload (MDO)
- **Writes trace data to TraceRAM**
- **Houses trace control registers and logic**

TraceRAM

- **Circular buffer**
  - ensures maximum trace window size
- **32-bit interface**
  - four AUX width read or write in a cycle
- **Configurable size**
  - 512B to 256KB
- **Trace data read-out through JTAG interface**
  - no effect on chip pin count


File Edit Refactor Navigate Search Project Tools Run Window Help
P: HelloWorld C: DC_B_232L T: Debug Build Active Run Profile Debug Trace
Timeline
Displayed tracefile: /HelloWorld/bin/DC_B_232L/TraceInfo/Debug/HelloWorl
Trace Flow
main
Function Name Address Start count
main d0000b9c 2
Trac...
HelloWorld
bin
DC_B_232L
TraceInfo
Debug
main.c
printf.c
#include <stdio.h>
int main(int argc, char **argv)
{
printf("Hello World\n");
}
Trace Disassembly
Raw Trace
Trace Capture
Help
Stop trigger
Address / Symbol: printf
Range mask: 0x0 - mask lower 0 bits
Range - Lower: printf
Range - Upper: printf
Fires when PC is inside masked range
Continue for 100 countdown units
Countdown unit byte instruction
Sync period 1 every 256
Save Trace
Trace file: tracefile1
Advanced triggers
Stop trigger on Cross Trigger Input Off
Stop trigger on Processor Trigger Input Off
Drive Cross Trigger Out Off
Drive Processor Trigger Out Off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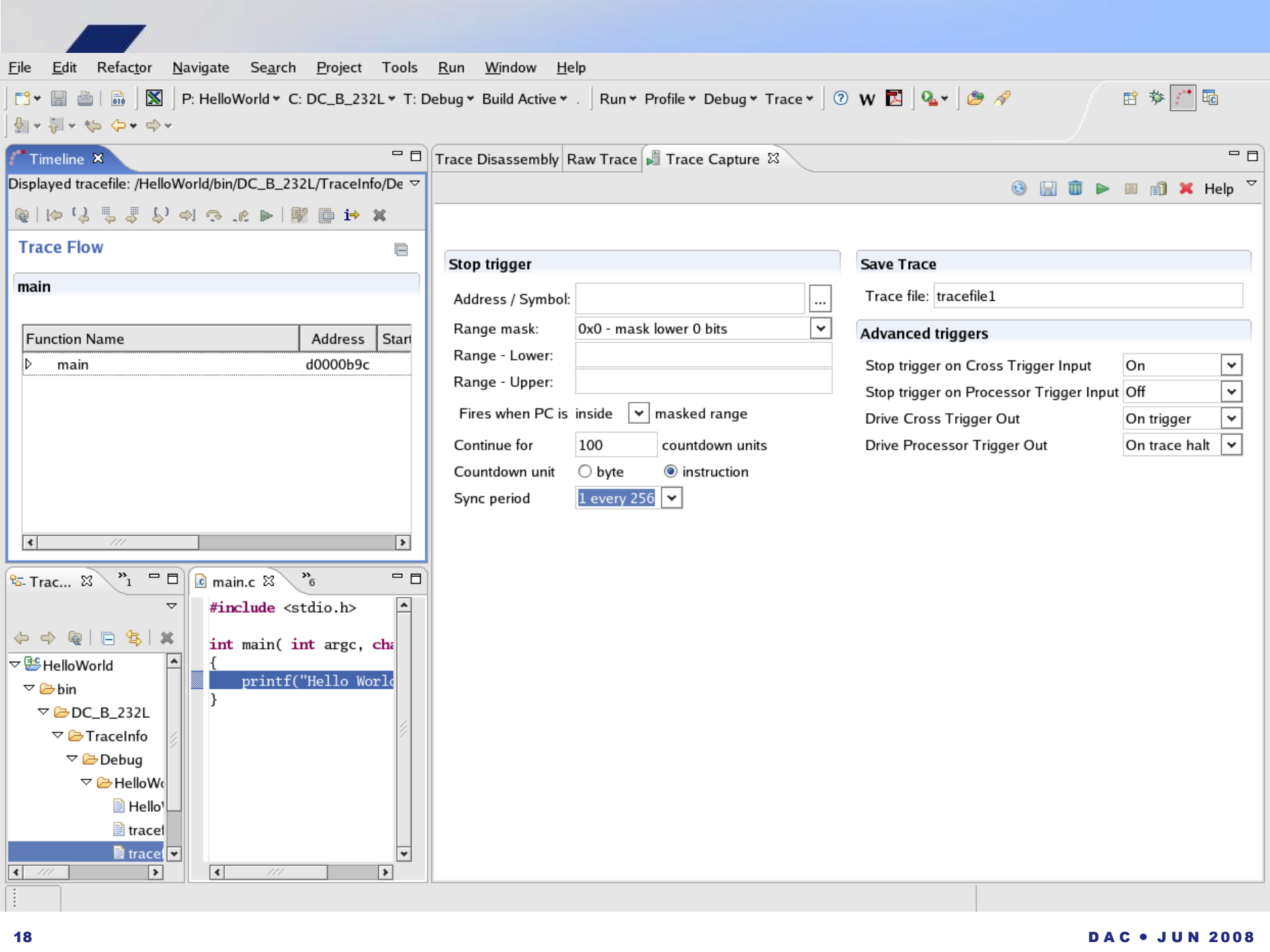
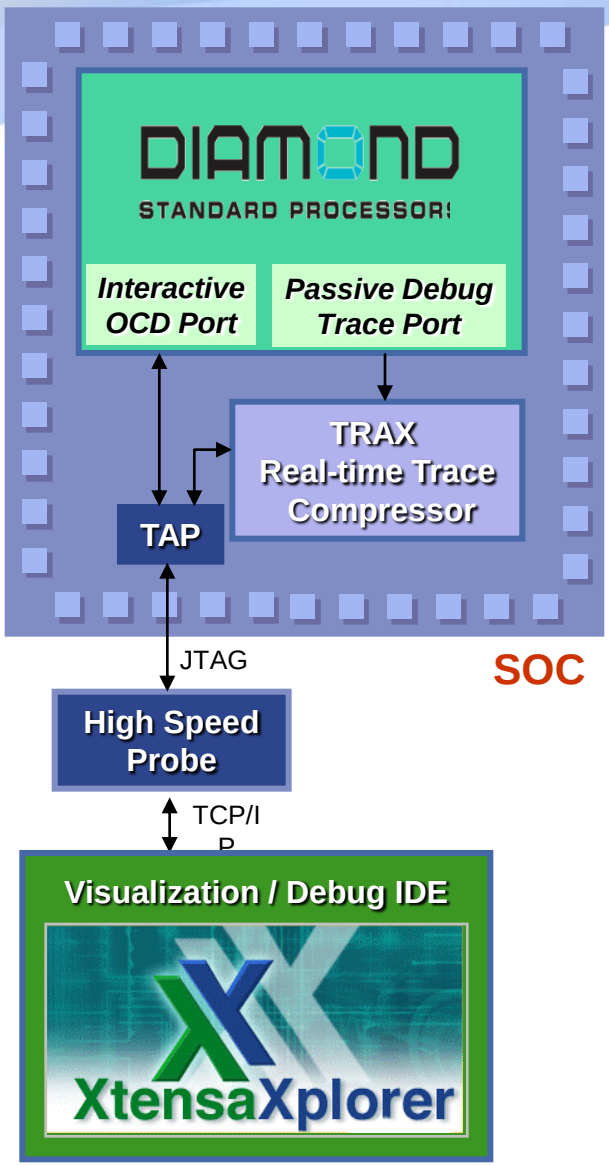
P: HelloWorld C: DC_B_232L T: Debug Build Active Run Profile Debug Trace
Timeline
Displayed tracefile: /HelloWorld/bin/DC_B_232L/TraceInfo/Debug/HelloWorld_built_on_20(
Trace Flow
main
printf
Function Name Address Start count End cou
main d0000b9c 2 3
Debug exception in OCD mode 0 1 1
printf d0000c2c 4 25
vfprintf d0000d08 26 42
_WindowOverflow4 d0000000 27 31
_vfprintf_r d0000d28 43 95
_WindowOverflow8 d0000080 48 57
localeconv d0004574 64 82
_WindowOverflow8 d0000080 65 74
Trac...
HelloWorld
bin
DC_B_232L
TraceInfo
Debug
findfp.c
main.c
printf.c
printf(fmt, va_alist)
char *fmt;
va_dcl
#endif
{
int ret;
va_list ap;
_REENT_SMALL_CHECK_INIT (_stdout_r (_REEN
#ifdef _HAVE_STDC
va_start (ap, fmt);
#else
va_start (ap);
#endif
Trace Disassembly
Raw Trace
Disassembled Instructions
printf
Block 2
Block Address Instruction
/home/akilesh/test_trax/workspace/Hellc
printf
printf(fmt, va_alist)
char *fmt;
va_dcl
#endif
2 d0000c2 entry a1, 80
d0000c2 or a11, a2, a2
d0000c3 s32i a7, a1, 36
d0000c3 s32i a6, a1, 32
d0000c3 s32i.n a5, a1, 28
d0000c3 s32i.n a4, a1, 24
d0000c3 s32i.n a3, a1, 20
d0000c3 s32i.n a2, a1, 16
d0000c4 l32r a10, d00008f8 <_ResetVector_litera
d0000c4 addi a14, a1, 16
d0000c4 addi a12, a1, 48
d0000c4 movi.n a13, 4
d0000c4 s32i.n a13, a1, 8
d0000c4 s32i.n a12, a1, 0
d0000c4 s32i.n a14, a1, 4
int ret;
va_list ap;
_REENT_SMALL_CHECK_INIT (_stdo
#ifdef _HAVE_STDC

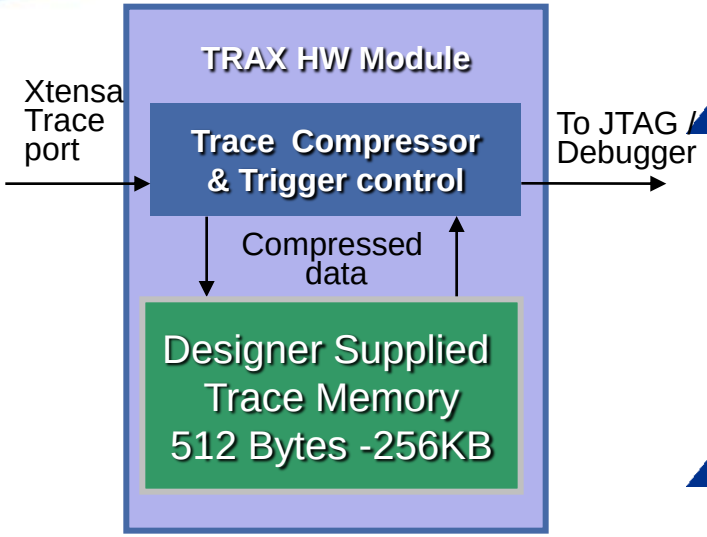

File Edit Refactor Navigate Search Project Tools Run Window Help
P: HelloWorld C: DC_B_232L T: Debug Build Active Run Profile Debug Trace
Timeline
Displayed tracefile: /HelloWorld/bin/DC_B_232L/TraceInfo/De
Trace Flow
main
Function Name
Address
Start
main
d0000b9c
Trac...
main.c
#include <stdio.h>
int main(int argc, cha
{
printf("Hello World
}
HelloWorld
bin
DC_B_232L
TraceInfo
Debug
Trace Disassembly
Raw Trace
Trace Capture
Help
Stop trigger
Address / Symbol:
Range mask:
0x0 - mask lower 0 bits
Range - Lower:
Range - Upper:
Fires when PC is inside masked range
Continue for
100
countdown units
Countdown unit
byte
instruction
Sync period
1 every 256
Save Trace
Trace file:
tracefile1
Advanced triggers
Stop trigger on Cross Trigger Input
On
Stop trigger on Processor Trigger Input
Off
Drive Cross Trigger Out
On trigger
Drive Processor Trigger Out
On trace halt

TRAX Overview



- **TRAX is a HW / SW solution for non-intrusive real- time trace debug**
- **Unparalleled Visibility into SoC**
  - Programmers can debug programs without interfering with program execution
- **Improves Developer Productivity**
- **Minimal silicon area requirements due to buffer compression**
  - Design-selected trace buffer depth for optimal visibility/cost tradeoff balancing
- **IEEE-ISTO Nexus 5001 compatible**
- **Available for both Tensilica Xtensa configurable and Diamond Standard processors**

TRAX Features

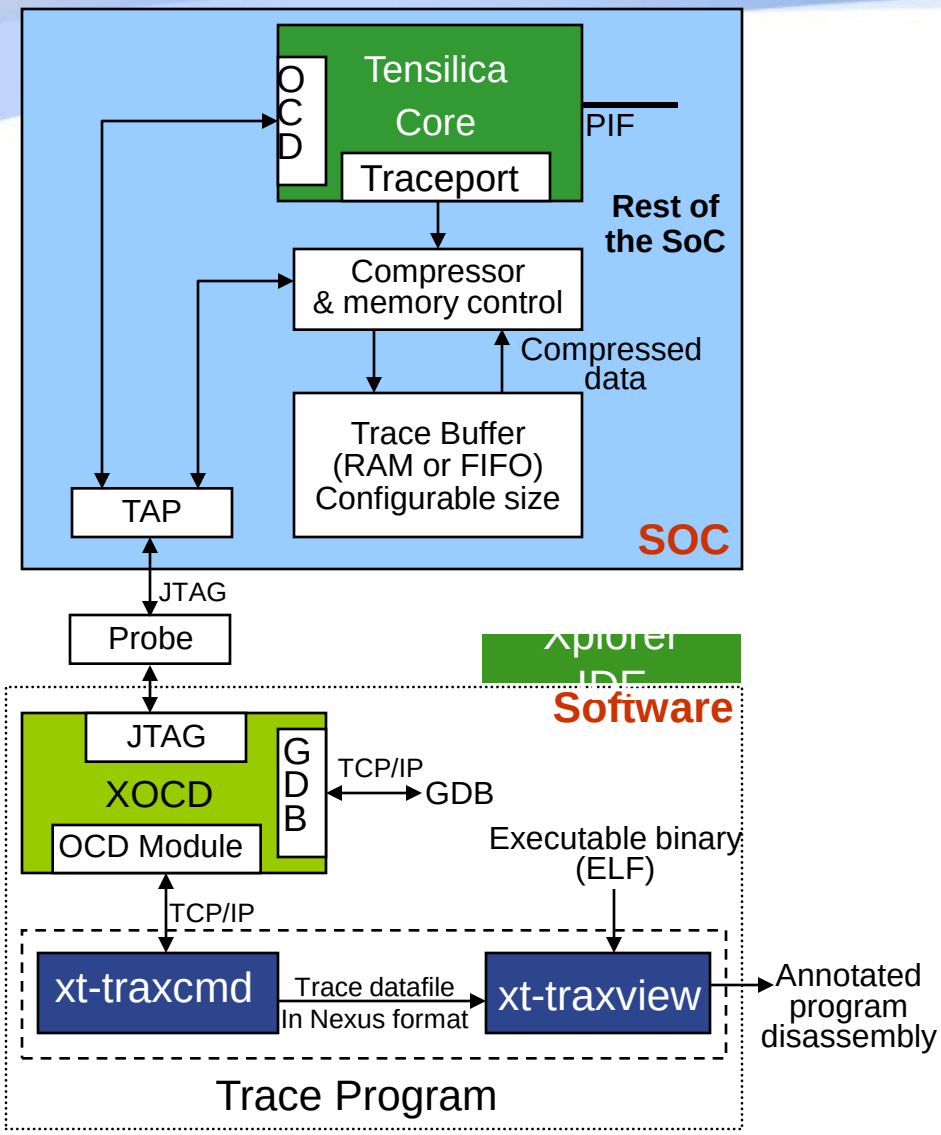


- **Program Counter based instruction trace**
- **On chip compression technology achieves < 1 bit per sample**
  - Minimal memory required = tiny silicon footprint
  - Rapid download speeds
- **User-configurable memory sizes depending on trace depth needs**
  - 512 bytes to 256 KB
- **Flexible Triggering mechanisms**
- **Debug and Trace software execution within the Xtensa Xplorer IDE**
  - Analyze and display the annotated disassembly of the program

TRAX Specifications

- **Traces all changes in program flow ("PC" = program counter)**
  - Including exceptions and interrupts
- **Uses circular on-chip trace buffer to capture trace stream**
  - User-supplied trace buffer
    - User can implement buffer as RAM or FIFO
  - Configurable trace memory size from 512 bytes to 256 KB
  - Approx 1000-2000 instructions traced per KB of trace memory
    - Employs trace compression (varies with code set)
- **Accepts PC-based triggers and external trigger event inputs (see later slide)**
- **Software tools convert compressed trace into an annotated program disassembly**
- **Graphical software tools to display trace data and perform debugging**

TRAX: HW+SW Conceptual Diagram



- **Compressed data communicated off-chip via TAP controller**
- **xt-traxcmd**
  - Controls trace compression hardware
  - Accepts triggering commands
  - Connects to XOCD
  - Produces trace data file
- **xt-traxview**
  - Reads in executable binary (ELF) and trace data file
  - Decompresses trace
  - Prints out disassembled program
- **Trace GUI inside Xplorer IDE**

Triggering Mechanisms

- **User can**
  - Set a stop trigger via PC address or address range
  - Manually stop execution by executing stop trigger
  - Set the amount of trace to capture after a stop trigger
- **Trace Compressor hardware has two external inputs and outputs**
  - Enable cross triggering between processors and other RTL blocks

TRAX Deliverables

- **Hardware deliverables**
  - TRAX RTL to connect to the trace port of a Diamond Standard Processor or Xtensa configurable processor
    - Compression and trigger logic: approx. 9000 gates
    - Trace buffer size is user-configurable
      - User must connect a RAM or FIFO for the Trace Buffer
  - EDA scripts to integrate with processor

- **Software components**
  - GUI-based tools integrated into Xplorer IDE