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Nexus – Makin' Multi- Core Work

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The Heisenberg Principle (1927)

“The act of observation disturbs the object observed in such unpredictable and uncontrollable ways that we are forever destined to be uncertain about the appearance of reality.”



Werner Karl Heisenberg
(1901 – 1976)
Würzburg, Germany

Problem Statement for Nexus

- How to trace a high performance 32-bit **Multi-Core** processor without affecting the system performance and to avoid the **Heisenberg Principle**?
- How to make a quantum leap forward with advanced debug tools?
- How to bring organization to a chaotic tools ecosystem?
 - Maximize tools reuse across multiple development cycles
 - Leverage multiple architectures in multiple markets
 - Minimize tool investments by the end user and development cost by the silicon and development tools companies



Nexus Overview

Nexus Forum Mission:

To solve the tools interface question permanently, through a standard that can evolve as required

To make Nexus the obvious solution for real-time Multi-Core debug and calibration.



Nexus a Quick History

- **1997**
 - 1H97: Automotive OEM/Tier1's requesting development tool interface enhancements
 - 2H97: Joint study with HP and Motorola SPS (now Freescale) – White Paper published
- **1998**
 - April: Nexus consortium formed (5 founding members)
 - 2Q: Conducted world-wide town-hall meetings with development tool and automotive industry
 - 3Q-4Q: Customer feedback and refine the specification
- **1999**
 - 19 member companies in the Nexus Consortium
 - Release of V1.0 of the Nexus 5001 Specification
- **2002**
 - First MCU demonstrates Nexus debug capabilities
 - Acceptance of the Nexus 5001 Forum By-Laws
- **2003**
 - Release of V2.0 of the Nexus 5001 Specification
- **2004**
 - Endorsement of the Standard by GM, Ford, Visteon, Motorola Automotive Group (now Continental) and Delphi
- **2007**
 - Joint partnership with OCP-IP Working Group

Nexus Philosophy

- **Aggregate Best Practices**
 - Proven functionality
 - Re-use technology where possible
- **Maximum functionality for minimum pins and silicon**
- **Move from 80+ pins to 2 to 20 pins while providing visibility that exceeds all other interfaces**
- **Minimal impact to performance while running**
- **Create visibility for information that is no longer available naturally**
- **Allow for vendor differentiation and extensions**
 - Structured vendor specific extensions without interfering with standard functionality



Scope of ISTO Nexus 5001™ Forum

Mission Statement:

To rapidly define a global, open, embedded processor development interface standard for embedded control applications.

- **RTOS Support and Analysis**
- **Real Time Debugging**
- **Hardware in the Loop**
- **Program Tuning**
- **Logic Analysis**
- **Run Control**
- **Prototyping**



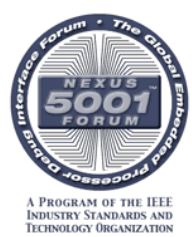
Development Tool
Standard Focus

Low Level API

Mechanical Interconnect

Silicon

www.nexus5001.org



Nexus Technology CPU Core List

Supported Clients:

- ❖ ARM7™
- ❖ ARM9™
- ❖ StarCore® DSP
- ❖ Video processor
- ❖ M-CORE
- ❖ Super10
- ❖ Power Architecture™ technology
 - ❖ MPC500
 - ❖ e200z6 Book-e
 - ❖ e200z3 Book-e
 - ❖ e200z1 Book-e
 - ❖ e200z0 Book-e
- ❖ Time Processor (eTPU)
- ❖ AHB (ARM AMBA bus)
- ❖ CompactRISC CR16C



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Nexus 2007 Membership



Nexus Benefits

MPU Vendors

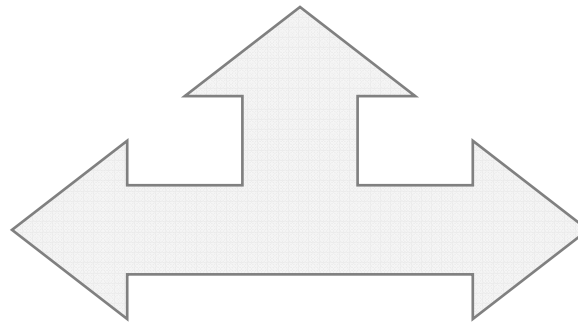
- Simplifies tools support
- Customer understanding of tools strategy
- Design re-use reduces time and cost
- Leverage best in-class tools
- Easier, faster check-out of tools on new architectures
- Ability to add features in standard method
- Same MCU in development and production
- Trace without the bus (pin overhead)

Users

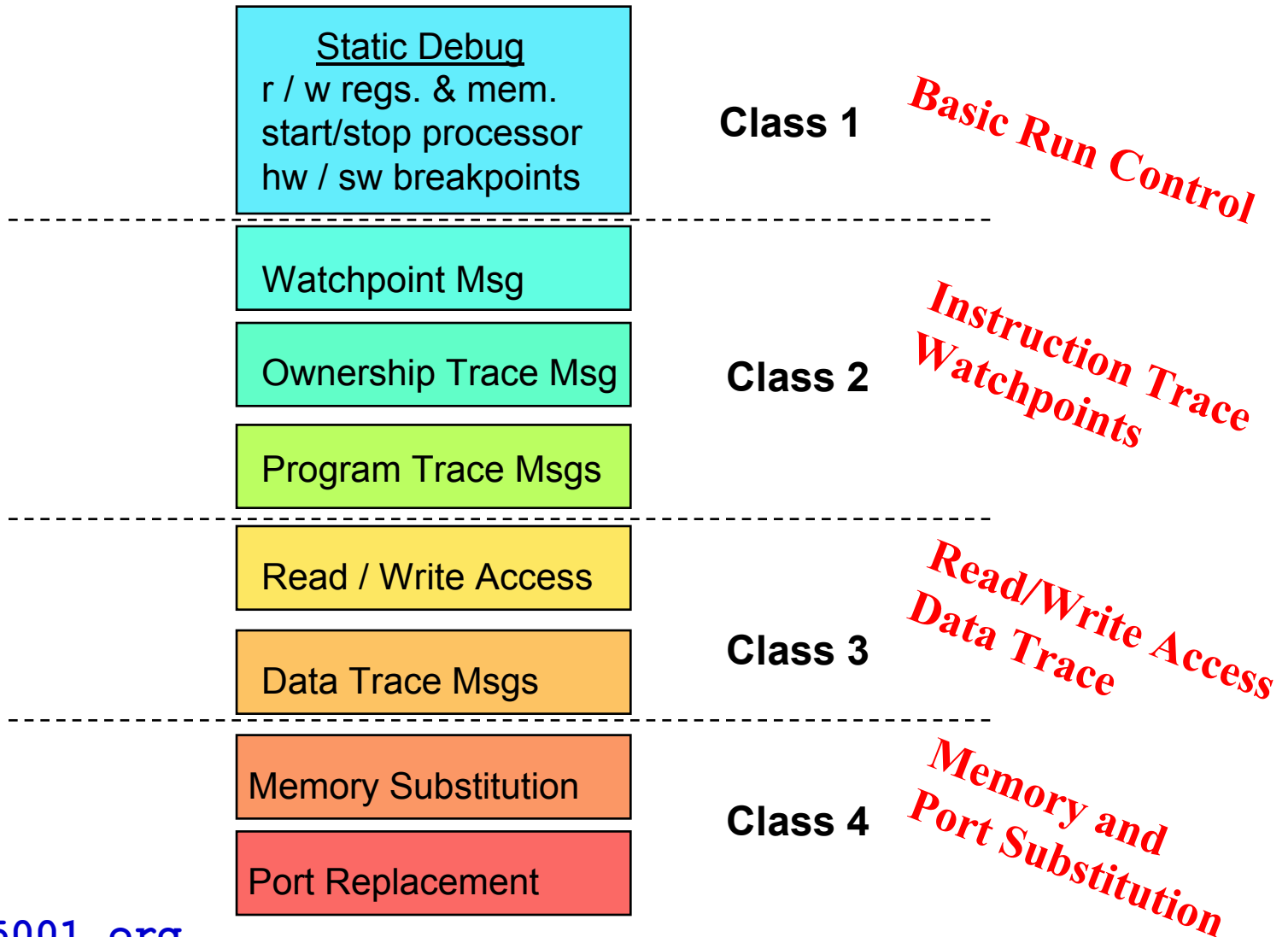
- Learning cycles – tools and architecture(s)
- Quicker time to market
- Development tool reuse
- Proven capabilities - multiple architectures
- Single small foot print interface
- Non-stop debugging, triggering and trace

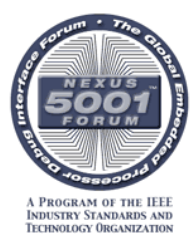
Tool Vendors

- Reduced development cost
- Rapid migration to new architectures
- Standard functions
- Opportunity to differentiate tools
- Opportunity to address customer requirements
- High performance – lower cost tools



Nexus Classes of Features





Nexus Compliance Classifications

Class 1

- Read/ write user registers in debug mode
- Read/ write user memory in debug mode
- Enter a debug mode from reset
- Enter a debug mode from user mode
- Single step instructions in user mode and re-enter debug mode
- Stop program execution on instruction/ data breakpoint and enter debug mode (minimum 2 breakpoints)
- Ability to set breakpoints or watchpoints
- Device identification
- Ability to send out an event occurrence when watchpoint matches

Class 2

- All class 1 features
- Monitor process ownership while process runs in real-time
- Monitor program flow while processor runs in real-time
- Full duplex mode (i. e., separate input and output ports)



Nexus Compliance Classifications (cont)

Class 3

- All class 2 features
- Monitor data writes while processor runs in real-time
- Read/ write memory locations while processor runs in real-time

Class 4

- All class 3 features
- Program execution (instruction/ data) from Nexus port (memory substitution)
- Ability to start traces upon watchpoint occurrence

Optional Features

- Ability to start memory substitution upon watchpoint occurrence
- Monitor data reads while processor runs in real-time
- LSIO port replacement and HSIO port sharing
- Transmit data values for acquisition by tool (data acquisition)

An interface is class 1, class 2, class 3, or class 4 compliant



Nexus Advantages

Key Advantages

- 23 Member Companies (2007)
- Started in 1998 to build a real-time MCU Interface Standard
- Only hard real-time Debug/Calibration/Hardware-in-the-loop interface
- **Multi-processor debug** support over a single interface
- Implemented on multiple CPU Architectures – 14 architectures
- Packet based interface
 - Provides a common protocol across multiple silicon providers
 - Packet format supports compression of address
- Branch Target Messaging to reduce the interface traffic
- High-speed development interface (500Mbps typical)
- Renewed cycles of learning – silicon, tools, development engineers



Nexus Technology Establishes Industry “Firsts”

Technology Firsts

- Proven on multiple CPU architectures – 30 MCUs and counting
- Multi-processor element interface
 - First Dual core device announced in October 2000
 - 5 client trace device announced in October 2004
- Packet-based standard protocol interface
- **Highest-speed debug interface** on any embedded MCU
- Low pin count – high function trace interface
- Proven debug and calibration interface has been proven out in the worlds most rugged embedded environments
- Version 2.0 of the specification released December 2003
- More than **150 million** units shipped with Nexus Class 2 and 3 ports

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Thank You

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